IN THE CLAIMS:

Claims 1, 3, 10, 13, 17, 22, 24, 31, 34 and 38 have been amended herein. All of the pending claims 1 through 42 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently Three Times Amended) A dynamic random access memory array located on a silicon substrate, said array comprising:

a plurality of memory cells, each memory cell including a field-effect access transistor and a stacked capacitor, each field-effect transistor having a first source/drain region functioning as a storage-node junction, each first source/drain region directly connected to the capacitor of each memory cell, each field-effect transistor having a second source/drain region functioning as an access-node junction, having an insulated gate having a lower surface overlying the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having vertical sidewalls, said upper surface and said sidewalls being covered by a first dielectric material layer;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening penetrating the interlevel dielectric layer and terminating at an access-node junction, each of said contact openings being self-aligned to the first dielectric material layer, each contact opening being lined with a layer of titanium metal and a layer of CVD titanium nitride located thereover and filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

2. (Previously Amended) The dynamic random access memory array of claim 1, wherein at least a portion of the titanium metal which overlies each access-node junction has reacted with silicon atoms on a surface of each access-node junction to form titanium silicide.

3. (Currently Three Times Amended) A dynamic random access memory cell array located on a silicon substrate, said array comprising:

a plurality of word lines, at least one of said plurality of word lines having a lower surface dielectrically insulated from the substrate by at least one silicon dioxide layer, said plurality of word lines each having an upper surface and sidewalls covered by a layer of silicon nitride;

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a capacitor for each memory cell of said dynamic random access memory cell array, each capacitor for storing a charge, the charge stored within each capacitor being accessible by at least one word line of said plurality of word lines;

an interlevel dielectric layer covering the memory cell array and the capacitors thereof;

a plurality of contact openings, each contact opening of the plurality of contact openings penetrating the interlevel dielectric layer to a junction in the substrate, each junction being covered by a titanium silicide layer and located adjacent at least one word line of the plurality of word lines, each contact opening of said plurality of contact openings at least partially overlapping the silicon nitride layer on the sidewall of said at least one adjacent word line, each of said contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug;

a plurality of digit lines formed on the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

4. (Previously Amended) The memory cell array of claim 3, wherein each capacitor comprises a stacked configuration.

5. (Previously Amended) The memory cell array of claim 3, wherein each contact opening of said plurality of contact openings, except in an area of the junction, further includes a lining of a titanium metal layer which is in contact with the titanium nitride layer, but not in contact with the tungsten plug that is within each contact opening.

6. (Previously Amended) The memory cell array of claim 3, wherein each contact opening of said plurality of contact openings includes a lining of a titanium metal layer in contact with the titanium nitride layer, but not in contact with the tungsten plug within each contact opening, said titanium metal layer overlying the titanium silicide layer in an area of the junction.

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7. (Previously Amended) The memory cell array of claim 3, wherein each word line of said plurality is insulated from the substrate along a portion of its length by a gate oxide layer and along a remainder of its length by a field oxide layer.

8. (Previously Amended) The memory cell array of claim 3, wherein each word line of said plurality comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion thereover.

9. (Previously Amended) The memory cell array of claim 3, wherein each word line of said plurality functions as a gate of a field effect cell access transistor for portions of its length where it traverses a gate oxide layer, each access transistor coupling a cell capacitor to a digit line of the plurality.

10. (Currently Three Times Amended) A dynamic random access memory on a silicon substrate, said memory comprising:

an array of memory cells, each memory cell of said array including a field-effect access transistor and a stacked capacitor, each transistor having a first source/drain region forming a storage-node junction, each first source/drain region being coupled to the capacitor of each memory cell, each transistor having a second source/drain region forming an access-

node junction, each transistor having an insulated gate having a lower surface overlying the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having generally vertical sidewalls, said upper surface and said sidewalls being covered by a first dielectric material;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array of memory cells to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening extending through the interlevel dielectric layer and terminating at an access-node junction, each digit line contact opening of said plurality of digit line contact openings self-aligned to the first dielectric material, each contact opening lined with a titanium metal layer, lined with a CVD titanium nitride layer, and filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least 2.5.

11. (Previously Amended) The dynamic random access memory of claim 10, wherein said second dielectric material is selectively etchable with respect to said first dielectric material.

12. (Previously Amended) The dynamic random access memory of claim 11, wherein at least a portion of the titanium metal which overlies each access-node junction has reacted with silicon atoms on the surface of each access-node junction to form titanium silicide.

13. (Currently Three Times Amended) A dynamic random access memory fabricated on a silicon substrate, said memory comprising:

an array of memory cells, each memory cell of said array of memory cells including a stacked capacitor and a field-effect access transistor having a gate electrode overlying the substrate, said gate electrode being dielectrically insulated from the substrate by a gate dielectric layer, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer formed from a second dielectric material selectively etchable with respect to said first dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening of said plurality of contact openings penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping said first dielectric material coating, each contact opening of said plurality of contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; [and]

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a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5..

14. (Previously Amended) The dynamic random access memory of claim 13, wherein each contact opening of said plurality of contact openings, except in an area of the region of the substrate, is lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within each contact opening.

15. (Previously Amended) The dynamic random access memory of claim 13, wherein each contact opening of said plurality of contact openings is lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within each contact opening, said titanium metal layer overlying the titanium silicide layer in an area of the region of the substrate.

16. (Previously Amended) The dynamic random access memory of claim 13, wherein each gate electrode comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion above the lower portion.

17. (Currently Three Times Amended) A dynamic random access memory on a silicon substrate, said memory comprising:

an array of stacked-capacitor memory cells, each memory cell of said array of memory cells having a field-effect access transistor with a channel formed in the substrate and a gate electrode overlying the substrate, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer formed from a second dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping the first dielectric material coating on the sidewalls of each gate electrode, each of said contact openings being lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

18. (Original) The dynamic random access memory of claim 17, wherein said second dielectric material is selectively etchable with respect to said first dielectric material.

19. (Previously Amended) The dynamic random access memory of claim 17, wherein each contact opening of said plurality of contact openings, except in an area of the region of the substrate, is lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within each contact opening.

20. (Previously Amended) The dynamic random access memory of claim 17, wherein each contact opening of said plurality of contact openings is lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within each opening,

said titanium metal layer overlying the titanium silicide layer in an area of the region of the substrate.

21. (Previously Amended) The dynamic random access memory of claim 17, wherein each gate electrode comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion above the lower portion.

22. (Currently Three Times Amended) A memory array on a silicon substrate comprising:

a plurality of memory cells, each memory cell including a field-effect access transistor and a stacked capacitor, each field-effect access transistor having a first source/drain region as a storage-node junction, each first source/drain region directly connected to the stacked capacitor of each memory cell, each field-effect access transistor having a second source/drain region as an access-node junction, each field-effect access transistor having an insulated gate having a lower surface overlying said silicon substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having vertical sidewalls, said upper surface and said sidewalls covered by a first dielectric material layer;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing said memory array at a level above that of at least one capacitor;

a plurality of digit line contact openings, each contact opening penetrating the interlevel dielectric layer and terminating at an access-node junction, each of said contact openings being self-aligned to the first dielectric material layer, each contact opening being lined with a layer of titanium metal and a layer of CVD titanium nitride thereabove and filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

23. (Previously Amended) The memory array of claim 22, wherein at least a portion of the titanium metal which overlies each access-node junction has reacted with silicon atoms on a surface of each access-node junction to form titanium silicide.

24. (Currently Three Times Amended) A memory cell array on a silicon substrate comprising:

a plurality of word lines, at least one of said plurality of word lines having a lower surface dielectrically insulated from the substrate by at least one silicon dioxide layer, said plurality of word lines each having an upper surface and sidewalls covered by a layer of silicon nitride;

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a capacitor for each memory cell of said memory cell array, each capacitor for storing a charge, the charge stored within each capacitor being accessible by the at least one word line of said plurality of word lines;

an interlevel dielectric layer covering the memory cell array and the capacitors thereof;

a plurality of contact openings, each contact opening of the plurality of contact openings penetrating the interlevel dielectric layer to a junction in the substrate, each junction being covered by a titanium silicide layer and located adjacent the at least one word line of the plurality of word lines, each contact opening of said plurality of contact openings at least partially overlapping the silicon nitride layer on the sidewalls of said at least one adjacent word line, each of said contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug;

a plurality of digit lines formed on the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

25. (Previously Amended) The memory cell array of claim 24, wherein each capacitor comprises a stacked configuration.

26. (Previously Amended) The memory cell array of claim 24, wherein each contact opening of said plurality of contact openings, except in an area of the junction, further includes a lining of a titanium metal layer which is in contact with the titanium nitride layer, but not in contact with the tungsten plug that is within each contact opening.

27. (Previously Amended) The memory cell array of claim 24, wherein each contact opening of said plurality of contact openings includes a lining of a titanium metal layer in contact with the titanium nitride layer, but not in contact with the tungsten plug within each contact opening, said titanium metal layer overlying the titanium silicide layer in an area of the junction.

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28. (Previously Amended) The memory cell array of claim 24, wherein each word line of the plurality of word lines is insulated from the substrate along a portion of its length by a gate oxide layer and along a remainder of its length by a field oxide layer.

29. (Previously Amended) The memory cell array of claim 24, wherein each word line of the plurality of word lines comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion thereover.

30. (Previously Amended) The memory cell array of claim 24, wherein each word line of the plurality of word lines functions as a gate of a field-effect cell access transistor for portions of its length where it traverses a gate oxide layer, each access transistor coupling a cell capacitor to a digit line of the plurality of digit lines.

31. (Currently Three Times Amended) A memory array on a silicon substrate comprising:

an array of memory cells, each memory cell of said array including a field-effect access transistor and a stacked capacitor, each transistor having a first source/drain region as a storage-node junction, each first source/drain region being coupled to the capacitor of a memory cell, each transistor having a second source/drain region as an access-node junction, each

transistor having an insulated gate having a lower surface overlying the substrate and insulated therefrom by a gate dielectric layer, having an upper surface, and having generally vertical sidewalls, said upper surface and said sidewalls covered by a first dielectric material;

an interlevel dielectric layer comprising a second dielectric material, said interlevel dielectric layer blanketing the array to a level above that of the capacitors;

a plurality of digit line contact openings, each contact opening extending through the interlevel dielectric layer and terminating at an access-node junction, each digit line contact opening of said plurality of digit line contact openings self-aligned to the first dielectric material, each contact opening lined with a titanium metal layer, lined with a CVD titanium nitride layer, and filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

32. (Previously Amended) The memory array of claim 31, wherein said second dielectric material is selectively etchable with respect to said first dielectric material.

33. (Previously Amended) The memory array of claim 32, wherein at least a portion of the titanium metal layer which overlies each access-node junction has reacted with silicon atoms on a surface of each access-node junction to form titanium silicide.

34. (Currently Three Times Amended) An access memory on a silicon substrate comprising:

an array of memory cells, each memory cell of said array of memory cells including a stacked capacitor and a field-effect access transistor having a gate electrode overlying the substrate, said gate electrode dielectrically insulated from the substrate by a gate dielectric layer, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer including a second dielectric material selectively etchable with respect to said first dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening of said plurality of contact openings penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region of said substrate covered by a titanium silicide layer, and each contact opening of said plurality of contact openings at least partially overlapping said first dielectric material coating, each opening of said plurality of contact openings lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

35. (Previously Amended) The access memory of claim 34, wherein each contact opening of said plurality of contact openings, except in the area of the junction, lined with a titanium metal layer contacting with the titanium nitride layer, but not contacting the tungsten plug within the contact opening.

36. (Previously Amended) The access memory of claim 34, wherein each contact opening of said plurality of contact openings lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within the opening, said titanium metal layer overlying the titanium silicide layer in the area of the junction.

37. (Previously Amended) The access memory of claim 34, wherein each word line comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion above the lower portion.

38. (Currently Three Times Amended) An access memory on a silicon substrate comprising:

an array of stacked-capacitor memory cells, each memory cell of said array of memory cells having a field-effect access transistor having a channel formed in the substrate and a gate electrode overlying the substrate, said gate electrode having an upper surface and sidewalls covered by a first dielectric material coating;

an interlevel dielectric layer including a second dielectric material, said interlevel dielectric layer blanketing the memory cell array;

a plurality of contact openings, each contact opening penetrating the interlevel dielectric layer to a region of the substrate contacting a single access transistor, said region covered by a titanium silicide layer, each contact opening of said plurality of contact openings at least partially overlapping the first dielectric material coating on the sidewall of a gate electrode, each of said contact openings being lined with a CVD titanium nitride layer and at least partially filled with a CVD tungsten plug; [and]

a plurality of digit lines formed on top of the interlevel dielectric layer, each digit line making electrical contact to each tungsten plug of a plurality of tungsten plugs; and

an aspect ratio of at least about 2.5.

39. (Previously Amended) The access memory of claim 38, wherein said second dielectric material is selectively etchable with respect to said first dielectric material.

40. (Previously Amended) The access memory of claim 38, wherein each contact opening of said plurality of contact openings, except in the area of the junction, lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within the contact opening.

41. (Previously Amended) The access memory of claim 38, wherein each contact opening of said plurality of contact openings lined with a titanium metal layer contacting the titanium nitride layer, but not contacting the tungsten plug within the opening, said titanium metal layer overlying the titanium silicide layer in the area of the junction.

42. (Previously Amended) The access memory of claim 38, wherein each word line comprises a doped polycrystalline silicon lower portion and a refractory metal silicide portion above the lower portion.

43. (New) The dynamic random access memory array of claim 1, wherein the aspect ratio is at least about 5:1.

44. (New) The dynamic random access memory array of claim 3, wherein the aspect ratio is at least about 5:1.

45. (New) The dynamic random access memory of claim 10, wherein the aspect ratio is at least about 5:1.

46. (New) The dynamic random access memory of claim 13, wherein the aspect ratio is at least about 5:1.

47. (New) The dynamic random access memory of claim 17, wherein the aspect ratio is at least about 5:1.

48. (New) The memory array of claim 22, wherein the aspect ratio is at least about 5:1.

49. (New) The dynamic memory cell array of claim 24, wherein the aspect ratio is at least about 5:1.

50. (New) The memory array of claim 31, wherein the aspect ratio is at least about 5:1.

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51. (New) The access memory of claim 34, wherein the aspect ratio is at least about 5:1.

52. (New) The access memory of claim 38, wherein the aspect ratio is at least about 5:1.